WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device, comprising a circuit block including a plurality of components,

wherein at least one of the plurality of components is supplied with a voltage having a value different from that supplied to the other component or components.

2. The semiconductor integrated circuit device of claim 1, including at least two power supplies for respectively supplying voltages having mutually different values to the circuit block,

wherein one of the power supplies is for supplying a predetermined voltage and the other power supplies are for respectively supplying voltages stepped down from the predetermined voltage in order.

3. The semiconductor integrated circuit device of claim 1, wherein each of the plurality of components is supplied with a voltage in accordance with a signal delay value caused under a given condition along a path to which said each of the components belongs.

4. The semiconductor integrated circuit device of claim 3, wherein at least one of the plurality of components which belongs to a path having a largest signal delay value is supplied with a voltage allowing the signal delay value of the path to be less than or equal to an admissible maximum signal delay value.

5. The semiconductor integrated circuit device of claim 3, wherein at least one of the plurality of components belonging to a path other than the path having the largest signal delay value is supplied with a voltage lower than the voltage supplied to the path

having the largest signal delay value.

6. The semiconductor integrated circuit device of claim 3, wherein at least two of the plurality of components belonging to an identical path are supplied with voltages having at least two values, based on the signal delay value.

7. The semiconductor integrated circuit device of claim 3, wherein if step-down of a voltage to be supplied to part of the components belonging to a first path is admitted based on the signal delay value, at least one of the plurality of components belonging to both of the first path and a second path is supplied with a voltage lower than a voltage supplied to the other component or components belonging to the first path.

8. The semiconductor integrated circuit device of claim 1, wherein the plurality of components are divided and placed in a plurality of regions corresponding to the values of voltages to be supplied to the respective regions.

9. The semiconductor integrated circuit device of claim 8, including a plurality of power supplies for respectively supplying voltages having mutually different values to the circuit block,

wherein each of the values of the voltages to be supplied to the respective one of the plurality of components is determined based on the number of the components supplied with the voltages from the power supplies.

10. The semiconductor integrated circuit device of claim 8, wherein at least one of a plurality of power lines connected to the respective ones of the plurality of components is

separated so that the regions corresponding to the values of the voltages to be supplied to the components are defined.

11. The semiconductor integrated circuit device of claim 8, wherein each of the plurality of components is placed in one of the regions, in accordance with a signal delay value caused under a given condition along a path to which said each of the components belongs.

12. The semiconductor integrated circuit device of claim 8, wherein at least two of the plurality of components belonging to an identical path are placed in at least two mutually different regions among the regions, based on a signal delay value caused under a given condition along a path to which each of the plurality of components belongs.

13. The semiconductor integrated circuit device of claim 8, wherein if step-down of a voltage to be supplied to part of the components belonging to a first path is admitted based on the signal delay value caused under a give condition along a path to which each of the plurality of components belong, at least one of the components belonging to both of the first path and a second path is placed in a region supplied with a voltage lower than a voltage supplied to a region in which the other component or components belonging to the first path is/are placed.

14. The semiconductor integrated circuit device of claim 8, wherein at least one of the regions is further divided into a plurality of regions in accordance with the distance from a power line.

15. The semiconductor integrated circuit device of claim 14, wherein the distance from the power line is a distance in which an IR-Drop effect is taken into consideration.

16. The semiconductor integrated circuit device of claim 14, wherein each of the plurality of components is placed in one of the further-divided regions, in accordance with a signal delay value caused under a given condition along a path to which said each of the components belongs.

17. The semiconductor integrated circuit device of claim 16, wherein at least one of the plurality of components belonging to a path having a maximum signal delay value is placed in a region which is nearest the power line among the further-divided regions.

18. The semiconductor integrated circuit device of claim 16, wherein at least one of the plurality of components belonging to a path having a signal delay value less than an admissible maximum signal delay value under a condition in which the component is placed in one of the further-divided regions, is placed in another region having a larger distance from the power line than said one of the further-divided regions such that the signal delay value of the path is less than or equal to the admissible maximum signal delay value.

19. The semiconductor integrated circuit device of claim 14, wherein the further-divided regions are further divided into a plurality of regions in accordance with the number of connection elements connected to the power line.

20. A method for designing a semiconductor integrated circuit device including a

circuit block with a plurality of components, wherein at least one of the plurality of components is supplied with a voltage having a value different from that supplied to the other component or components.

21. The method of claim 20, wherein a signal delay value caused under a given condition along a path to which each of the plurality of components belongs is calculated statistically, and

the smallest voltage among voltages at which the signal delay value of the path is less than or equal to an admissible maximum signal delay value is supplied as a voltage which is to be supplied to the components and has a magnitude less than or equal to the second largest value, based on the signal delay value.

22. The method of claim 20, wherein a signal delay value caused under a given condition along a path to which each of the plurality of components belongs is calculated, and

a value according to the signal delay value is supplied to each of the components.

23. The method of claim 22, wherein voltages having at least two values are supplied to at least two of the plurality of components belonging to an identical path, based on the signal delay value.

24. The method of claim 22, wherein if step-down of a voltage to be supplied to part of the components belonging to a first path is admitted based on the signal delay value, at least one of the components belonging to both of the first path and a second path is supplied with a voltage lower than a voltage supplied to the other component or

components belonging to the first path.

25. The method of claim 20, wherein a signal delay value caused under a given condition along a path to which each of the plurality of components belongs is calculated statistically, and

a plurality of regions corresponding to the values of voltages to be respectively supplied thereto are provided in the semiconductor integrated circuit device, based on the signal delay value.

26. The method of claim 25, wherein the value of a voltage to be supplied to each of the plurality of components is determined based on the number of the components to which voltages are supplied from a plurality of power supplies for respectively supplying mutually different voltages to the circuit block.

27. The method of claim 26, wherein at least one of a plurality of power lines connected to the respective ones of the plurality of components is separated so that the regions corresponding to the values of the voltages to be supplied to the respective components are defined.

28. The method of claim 25, wherein each of the plurality of components is placed in one of the regions, based on the signal delay value.

29. The method of claim 25, wherein at least two of the plurality of components belonging to an identical path are placed in at least two mutually different regions among the regions, based on the signal delay value.

30. The method of claim 25, wherein if step-down of a voltage to be supplied to part of the components belonging to a first path is admitted based on the signal delay value, at least one of the components belonging to both of the first path and a second path is placed in a region supplied with a voltage lower than a voltage supplied to a region in which the other component or components belonging to the first path is/are placed.

31. The method of claim 25, wherein at least one of the regions is further divided into a plurality of regions in accordance with the distance from a power line.

32. The method of claim 31, wherein the distance from the power line is a distance in which an IR-Drop effect is taken into consideration.

33. The method of claim 31, wherein a signal delay value caused under a given condition along a path to which each of the plurality of components belongs is calculated, and

each of the components is placed in one of the further-divided regions based on the signal delay value.

34. The method of claim 33, wherein one of the plurality of components belonging to a path having a signal delay value less than an admissible maximum signal delay value under a condition in which the component is placed in one of the further-divided regions, is placed in another region having a larger distance from the power line than said one of the further-divided regions such that the signal delay value of the path is less than or equal to the admissible maximum signal delay value.

35. The method of claim 33, a voltage to be supplied to a region in which at least one of the plurality of components belonging to a path having a signal delay value less than an admissible maximum signal delay value is placed is reduced by changing the number of connection elements in a power line to which the component is connected.